REMARKS

Claims 1-14 are pending in this application. By this Amendment, claims 1, 11 and 14 are amended.

I. Claim Rejection Under 35 U.S.C. §102(e) and 35 U.S.C. §103(a)

Claims 1-3, 9-10 and 12-14 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,784,557 to Nakamura et al. (hereinafter "Nakamura"); and claims 4-8 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakamura in view of U.S. Patent Application Publication No. 2001/0000116 to Shimizu et al. (hereinafter "Shimizu").

The Office Action asserts that Nakamura teaches a semiconductor device/electronic device and a method of manufacturing such device, comprising (in-part): a semiconductor substrate/wafer that includes an active element and an integrated circuit/IC chip having an active element in the active element region; electrodes electrically connected to the integrated circuit, the electrodes including a first electrode and a second electrode; a resin layer that is formed on a surface of the semiconductor substrate where the electrode is also formed, so as to avoid the electrode; a wiring layer that extends from the electrode and across the top of the resin layer, and includes a plurality of electrically connecting portion/wiring sections, the plurality of electrically connecting portions including a first electrically connecting portion electrically connected to the first electrode and a second electrically connecting portion electrically connected to the second electrode; and an external terminal that is provided on the electrically connected portions. The Office Action acknowledges that Nakamura fails to teach that the first electrically connecting portion being formed so as to cover nearly the entire top surface of the resin layer.

The Office Action goes on to rely on Shimizu and asserts that Shimizu teaches a device structure comprising electrode/external terminal connections having a variety of

wiring configurations including the configurations wherein the first electrically connecting portion/ground wiring section nearly/substantially covers the entire top surface of an underlying insulating/dielectric layer except for the area occupied by the second electrically connecting portion/wiring section and a portion surrounding the second electrically connecting portion/wiring section.

Nakamura and Shimizu do not disclose or suggest the feature "the surface area of the first electrically connecting portion being larger than the active element region," as recited in independent claims 1, 11 and 14 of the present invention. Specifically, Nakamura discloses the semiconductor device which has metal wirings (4) having different wiring length/area (Fig. 15a). However, Nakamura does not disclose the area where the active element region extends, so Nakamura does not disclose or suggest the feature "the surface of the first electrically connecting portion being larger than the active element region."

Shimizu discloses the semiconductor device having the ground wiring section (1003) nearly/substantially cover[s] the entire top surface of an underlying insulating/dielectric layer. However, Shimizu does not disclose the area where the active element region extends, so Shimizu does not disclose or suggest the feature "the surface area of the first electrically connecting portion being larger than the active element region."

Independent claims 1, 11 and 14 have been amended for clarification and to add the feature "the surface area of the first electrically connecting portion being larger than the active element region" (paragraphs [0033] and [0045]).

Based on the arguments presented above, independent claims 1, 11 and 14 are in condition for allowance. Therefore, dependent claims 2-10, 12-13 are also in condition for allowance. It is respectfully requested that the Examiner reconsider and withdraw the rejections.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-14 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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